IN THE SPECIFICATION

Please amend the appropriate paragraphs of specification in accordance with proposed changes as outlined hereinbelow:

Please amend the paragraph on pages 21 through 23, from numbered line 17 on page 21 to numbered line 16 on page 23, as follows:

The operation of the word line enabling circuitry of FIG. 7 can be described along with an examination of the waveform diagram in FIG. 8. In FIG. 8, an exemplary access is shown which illustrates the functionality of the circuits in FIG. 7. A write-read-write three-cycle consecutive access is performed on the same row address XADR A followed by a read access to a second row address XADR B and a write access to a third row address XADR C. On the first access, the row address XADR is presented to the decoder XDEC and the external write signal WE is asserted. Since the consecutive access signal CA is low since this is the first access, an assertion of the read clock RCK generates a high value of the read enable RE and the appropriate read word line RWL1 [WLR1] is driven high. The read cycle completes with the amplification of the read data line signal and the read data is stored in the column latch. At this point, the latch enable LTE is asserted and the set-reset latch SRL is triggered to store a high signal denoting a write access. The next access is a read access to the same row. Since the data is in the column latches and not in the cell array, the circuit must delay the write phase of the first access and not enable the read word line RWL1. This is accomplished by a logic-AND function of the read RE and write WE signals with the inverse of the CA signal. In other words, read word line RWL1 and write word line WWL1 activations are disabled on subsequent accesses to the same row. The column readout

circuitry described below will illustrate that the data is read from the column latches and not the cell array. The third access is a write to the same row address XADR A. Again, since the CA signal is asserted, the read word line RWL1 and write word line WWL1 are disabled and the data is written directly into the column latches. On the fourth access, the row address XADR changes and the consecutive access signal CA is deactivated. Since a high value is stored in the set-reset latch SRL, the circuit has recorded that a write access has occurred and the data in the column latches must be written into the memory array. As the write enable clock WCK is activated, the write word line WWL1 [WLW1] of the first row activates and begins the write phase of the third access. Simultaneously, the row address XADR B for the read phase of the fourth access is decoded and the read word line RWL2 is activated. The fifth cycle is a read access to the third address XADR C and begins with the assertion of the external read signal RE. The write phase of the previous write cycle begins with the activation of the write enable clock WCK and the write word line WWL2 of the second row is asserted. Simultaneously, on the rising edge of the read enable clock RCK, the read word line RWL3 [WLR3] of the third row is activated and the final read access is completed. This example illustrates how the minimal circuitry of FIG. 7 uses latches at each row to reduce the number of address decoders from two to one. In addition, this circuitry maintains the integrity of the data even when the current data is stored in the column latches by only accessing the memory array when the consecutive accesses are to distinct rows.

Please amend the paragraph bridging pages 25 and 26, from numbered line 7 on page 25 to numbered line 2 on page 26, as follows:

FIG. 10B shows exemplary access waveforms for the circuitry of FIG. 10A, in accordance with the second embodiment of the present invention. In the second embodiment, the memory is composed of a set of upper memory mats UMAT and lower memory mats LMAT. The cells are controlled by row signals including the read word lines URWL,LRWL

~~UWRL, LWRL~~ and the write word lines UWWL, LWWL. In addition, the mats are divided into columns of cells that are accessed through read data lines URDL, LRDL and write data lines UWDL, LWDL. In this embodiment, the upper read data line URDL and lower write data line LRDL are connected to a single sense amplifier SA circuit. The output of the sense amplifier SA is then connected to the input of the latch element LT that is controlled by the column latch signal LTI. The output of the latch can be connected to either the upper write data line UWDL or the lower write data line LWDL through a corresponding switch element, which are independently controlled by the upper latch output ULO and lower latch output LLO column signals. The advantage of this structure is that the number and area of peripheral circuits to the array mats can be reduced by sharing the sense amplifier and latch elements between a pair of mats. In this embodiment, the total area of the circuitry can be reduced versus the first embodiment.

Please amend the paragraph bridging pages 28 and 29, from numbered line 17 on page 28 to numbered line 2 on page 29, as follows:

FIG. 11B shows exemplary access waveforms for the circuitry of FIG. 11A, in accordance with the third embodiment of the present invention. A fundamental difference here from the first embodiment is that several latches are placed between the sense amplifier SA and the write data line <u>WDL</u> [WBL] instead of a single latch. With this configuration, the effective write access speed of the memory array can be increased versus that in the first embodiment. For a write phase that is several times slower than the read phase, the access speed of the first embodiment is limited to the speed of the write phase. In this embodiment, the effective access speed is limited to the speed of the faster read phase.